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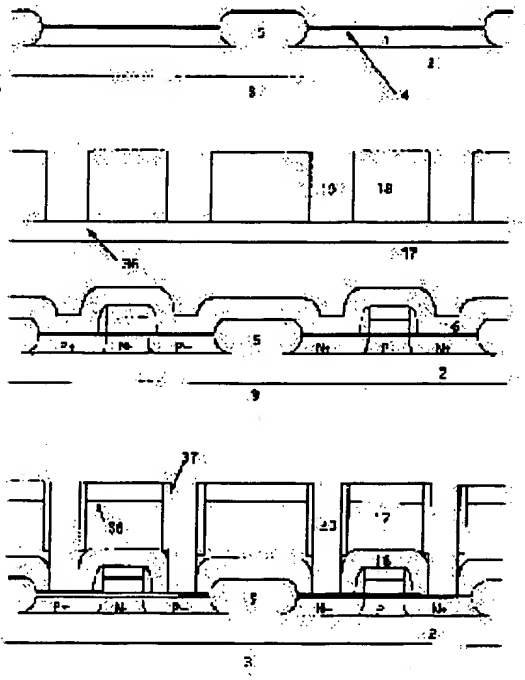
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the deterioration of an insulating film due to charging by providing a first charging film on the insulating film formed on a semiconductor element, providing holes in the first conducting film and the insulating film, forming a second conducting film on the sidewalls of the holes, then providing a hole in the insulating film in the conducting region of the semiconductor element.

SOLUTION: On a supporting substrate 3, an embedded oxide film 2 and a silicon film 1 are provided. An oxide film 4 is formed thereon. Then, the oxide film 4 in an element isolating region is removed by etching, and an oxide film 5 is formed. Thereafter, an non-doped silicate glass(NSG) film 16 and a boron phosphosilicate glass BPSG film 17 are formed by painting method. Then, after a TiN layer 36 is formed, resist 18 is formed thereon. A hole is opened in the resist 18, and a contact hole part 19 is formed. Furthermore, a contact hole 20 is opened in the BPSG film 17 and the NSG film 16 with the resist 18 as a mask.



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* NOTICES *

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2.**** shows the word which can not be translated.
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device including the dry etching process for taking contact to the semiconductor region and the conductive field in especially floating about the manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] As the manufacture approach of the semiconductor device using the conventional SOI substrate, the example which forms CMOS is explained below with reference to drawing 2 . As shown in drawing 7 (1), a SOI substrate is embedded on the support substrate 3, and has a silicone film 1 an oxide film 2 and on it. Since it is thick, in order to obtain SOI of high quality, this oxidizes the surface silicon layer 1 which forms a transistor, and it obtains the surface silicon layer of the support substrate 3 which is silicon by adjusting the thickness of the silicon layer 1 to 70nm using etching etc. while it forms a silicon layer further. The thickness of an oxide film 2 is 100nm here.
[0003] Subsequently, an oxide film 4 is formed in 10nm thickness by the oxidizing [thermally] method, the SIN film (not shown) is formed in the thickness of 100nm by LPCVD (low-temperature chemical vapor deposition), and the photolithography method and dry etching remove the SIN film of a component isolation region, and an oxide film 4. Next, it oxidizes thermally by the thickness of 160nm, the oxide film 5 for isolation is formed, and a heat phosphoric acid removes the SIN film (refer to drawing 7 (2)).
[0004] With the photolithography method and ion-implantation of a PMOS active region, the ion implantation of Lynn is carried out in impregnation energy 25KeV, and dose 5x1012 ion / cm2, and the high impurity concentration of the channel field 6 of PMOS is determined. Then, the ion implantation of the boron is carried out to an NMOS active region with the photolithography method and ion-implantation in impregnation energy 30KeV, and dose 5x1012 ion / cm2, and the high impurity concentration of the channel field 7 of NMOS is determined. Furthermore, HF removes an oxide film 4 1%, and gate oxide 8 is formed in the thickness of 7nm by the oxidizing [thermally] method. Then, the ion implantation of Lynn is carried out to the polish recon layer 9 with ion-implantation in impregnation energy 20KeV, and dose 5x1015 ion / cm2, the polish recon layer 9 is formed in the thickness of 150nm by the LPCVD method, and the WSi layer 10 is continuously formed in the thickness of 100nm with a CVD method. Then, the WSi layer 10 and the polish recon layer 9 are etched by the photolithography method and the dry etching method, and a gate electrode is formed (refer to drawing 7 (3)).
[0005] The ion implantation of BF2 is carried out to a PMOS active region with the photolithography method and ion-implantation in impregnation energy 20KeV, and dose 5x1013 ion / cm2, and the high impurity concentration of the drain buffer diffusion layer 11 of PMOS is determined. In addition, since it is referred to as the so-called LDD, this drain buffer diffusion layer 11 is established. Then, the ion implantation of Lynn is carried out to an NMOS active region with the photolithography method and ion-implantation in impregnation energy 15KeV, and dose 5x1013 ion / cm2, and the high impurity concentration of the drain buffer diffusion layer 12 of NMOS is determined. Since it is referred to as the

so-called LDD, this drain buffer diffusion layer is established. In order to use it, making the active-region section of PMOS and NMOS depletion-ize fundamentally, thickness is thinly formed in low concentration. Then, 150nm (not shown) of oxide films is formed with a CVD method, 140nm etchback of this oxide film is carried out by the dry etching method, and the sidewall 13 of an oxide film is formed in a gate electrode side attachment wall.

[0006] Then, the ion implantation of BF2 is carried out to a PMOS active region with the photolithography method and ion-implantation in impregnation energy 20KeV, and dose 5x1015 ion / cm2, and the source of PMOS and the high impurity concentration of the drain diffusion layer 14 are determined. Then, the ion implantation of Lynn is carried out to an NMOS active region by the photolithography method and the ion method in impregnation energy 15KeV, and dose 5x1015 ion / cm2, and the source of NMOS and the high impurity concentration of the drain diffusion layer 15 are determined (refer to drawing 7 (4)).

[0007] 150nm of NSG (non dope silicate glass) film 16 is formed by the applying method, and 750nm of BPSG (boron phosphorus silicate glass) film 17 is continuously formed by the applying method. Then, 900 degrees C, nitrogen-gas-atmosphere mind, and the impurity that performed heat treatment for 20 minutes and carried out the ion implantation with the reflow of the BPSG film 17 and the above are activated. Then, opening of the contact hole section 19 for connecting electrode wiring with a semiconductor device by the photolithography method is formed in a resist 18 (refer to drawing 7 (5)).

[0008] Next, the resist 18 which carried out opening of the contact hole section 19 is used as a mask, and opening of the contact hole section 20 is used to the BPSG film 17 and the NSG film 16. At this time, the etching system is impressing high-frequency power also to a wafer maintenance electrode with the inductive-coupling mold plasma etching system. Etching conditions are C2F6 flow-rate 50sccm, degree of vacuum 5mTorr, source impression power 2500W, and wafer maintenance electrode impression power 800W, and the amount of over etching is made into 30% to the deepest source drain contact section. In addition, this over etching makes [more] etching time so that all contacts may be formed in consideration of variation to just etching (refer to drawing 8 (6)). Then, a resist 18 is removed.

[0009] Next, a TiN layer is continuously formed Ti layer in the thickness of 60nm and formed in the thickness of 60nm by the spatter with a spatter, and the barrier metal layer 21 is formed. Next, 22 [W-layer] is formed in the thickness of 500nm with a CVD method, etchback of 22 [W-layer] is carried out by the dry etching method after that, and it leaves 22 [W-layer] only to the contact hole section 20. Next, etchback of the barrier metal layer 21 is carried out by the dry etching method, and it leaves the barrier metal layer 21 only to the contact hole section 20. next, a spatter -- the AlCu layer 24 (0.5% of Cu concentration) is formed in the thickness of 400nm, and the TiN layer 25 is formed in the thickness of 80nm for the TiN layer 23 at the thickness of 80nm, respectively. Then, the TiN layer 25, the AlCu layer 24, and the TiN layer 23 are etched into an electrode circuit pattern by the photography method and the dry etching method, and electrode wiring is formed (refer to drawing 8 (7)).

[0010] Subsequently, SiO2 film 26 is formed in 2-micrometer thickness by the plasma-CVD method, and flattening of the SiO2 film 26 is continuously carried out by the CMP method (chemical mechanical-polishing method). At this time, the thickness of SiO2 film is on electrode wiring, and may be 1 micrometer. Next, opening which is the hole section (veer hole section) 28 which connects electrode wiring and up wiring by the photolithography method is formed in a resist 27 (refer to drawing 9 (8)). The resist 27 which carried out opening of this veer hole section 28 is used as a mask, and opening of the hole (veer hole) 29 is used to SiO2 film 26 by dry etching. At this time, an etching system is an inductive-coupling mold plasma etching system, and is impressing high-frequency power also to a wafer maintenance electrode. The etching condition makes the amount of over etching 50% by C2F6 flow-rate 50sccm, degree of vacuum 5mTorr, source impression power 2500W, and wafer maintenance electrode impression power 800W (refer to drawing 9 (9)). Then, a photoresist 27 is removed.

[0011] Next, Ti layer is formed in 60nm thickness by the spatter, a TiN layer is continuously formed in 60nm thickness by the spatter, and the barrier metal layer 30 is formed. Next, 31 [W-layer] is formed in

the thickness of 500nm with a CVD method, the etching back of 31 [W-layer] is carried out by the dry etching method, and it leaves 31 [W-layer] only to the veer hole section 29. Next, the etching back of the barrier metal layer 30 is carried out by the dry etching method, and it leaves the barrier metal layer 30 only to the veer hole section 29. Furthermore, the TiN layer 32 is formed in the thickness of 80nm by the spatter, it continues, and the AlCu layer 33 (0.5% of Cu concentration) is formed in the thickness of 800nm, and the TiN layer 34 is further formed in the thickness of 80nm, respectively. Then, by the photolithography method and the dry etching method, the TiN layer 34, the AlCu layer 33, and the TiN layer 32 are etched, and up electrode wiring is formed. Then, the SiN layer 35 of the passivation film is formed in the thickness of 600nm by the plasma-CVD method (refer to drawing 10 (10)). Then, opening of the bonding pad connection hole is carried out to the SiN layer 35 by the FORI lithography method and the dry etching method.

[0012]

[Problem(s) to be Solved by the Invention] In manufacture of LSI to which detailed-ization progresses, the contact hole which connects metal wiring with a semiconductor device, and the veer hole which connects up metal wiring and lower metal wiring are formed by using and processing dry etching into an interlayer insulation film etc. In the dry etching, the side attachment wall of a hole is charged in negative with the random electron of the movement direction, and the amount of the electron which flows into a hole as a result decreases. On the contrary, since directivity of a cation is high, an inflow into a hole does not change, but as a result, a hole pars basilaris ossis occipitalis is just charged. The inclination becomes remarkable as detailed-izing and high aspect-ization progresses. In the case of a SOI device, if a hole pars basilaris ossis occipitalis is charged, the potential difference will occur between an active region and a support substrate, and the embedding oxide film which exists between them will deteriorate. The dependability of LSI and the yield fall for degradation of the embedding oxide film.

[0013] This invention aims at offering the manufacture approach of the possible semiconductor device of preventing degradation of the insulator layer by electrification in the case of dry etching.

[0014]

[Means for Solving the Problem] In the manufacture approach of a semiconductor device that the manufacture approach of the semiconductor device of this invention uses a SOI substrate The process which forms an insulator layer on wiring which connects a semiconductor device or it, and forms the 1st conductive film subsequently to the insulator layer top, Opening is carried out to extent which does not reach said the 1st conductive film and said insulator layer by etching at the conductive field of said semiconductor device, or said wiring. The 2nd conductive film is formed in the side attachment wall of the account opening of back to front. It is characterized by having the process which forms a hole by carrying out opening of the conductive field of said semiconductor device, or said insulator layer after said wiring by dry etching in the condition of having made it flowing through the 2nd conductive film electrically with said 1st conductive film.

[0015] after the manufacture approach of the semiconductor device of this invention is desirable and formation of said hole etches said 1st conductive layer into a mask for the photoresist formed on said 1st conductive film -- this photoresist -- removing -- continuing -- this -- the 1st conductive film can be performed on a mask by carrying out dry etching of said insulator layer.

[0016] In what has the process which carries out opening of the contact hole for the manufacture approach of the semiconductor device of this invention to form ********** to the semi-conductor or the conductive field by which insulating separation was carried out spatially to an insulating layer by plasma etching Said process is characterized by performing plasma etching until it arrives at said field, where a conductive layer is formed in the field which said insulating layer exposes including the side-attachment-wall section of opening which formed plasma etching by the stop and after that plasma etching before arriving at said field.

[0017] Preferably, the manufacture approach of the semiconductor device of this invention can have the process which removes said conductive layer by wet etching, after forming a contact hole according to said process.

[0018] An operation of this invention is explained below. Opening of the manufacture approach of the

semiconductor device of this invention is carried out to extent which does not reach said the 1st conductive film and said insulator layer by etching at the conductive field of said semiconductor device, or said wiring. From forming the 2nd conductive film in the side attachment wall of the account opening of back to front, and forming a hole by carrying out opening of the conductive field of said semiconductor device, or said insulator layer after said wiring by dry etching in the condition of having made it flowing through the 2nd conductive film electrically with said 1st conductive film Since the pars basilaris ossis occipitalis of a hole can reduce electrification of the pars basilaris ossis occipitalis compared with the former even if it reaches a conductive field or wiring, it is made to prevention of degradation by dielectric breakdown of the insulator layer of a SOI substrate with utility.

[0029] after [furthermore,] formation of said hole etches said 1st conductive layer into a mask for the photoresist formed on said 1st conductive film -- this photoresist -- removing -- continuing -- this -- a hole can be formed in self align from performing the 1st conductive film on a mask by carrying out dry etching of said insulator layer.

[0030] Moreover, it sets to the manufacture approach of the semiconductor device which carries out opening of the contact hole for forming the electrical installation to the semi-conductor or the conductive field by which insulating separation was carried out spatially to an insulating layer by etching. By performing plasma etching and forming a contact hole until it arrives at said field, where a conductive layer is formed in the field which said insulating layer exposes including the side-attachment-wall section of opening which formed etching by the stop and after that etching before arriving at said field Since electrification of the pars basilaris ossis occipitalis can be reduced compared with the former even if the pars basilaris ossis occipitalis of a contact hole arrives at a semi-conductor or a conductive field by plasma etching, it contributes to being able to mitigate the bad influence to layers, such as an insulating layer by electrification, and preventing degradation of the property of equipment.

[0031] Furthermore, after forming a contact hole, compared with dry etching, the bad influence to the substrate of the lower part of the contact hole can be reduced by removing said conductive layer by wet etching.

[0032]

[Embodiment of the Invention] In the manufacture approach of a semiconductor device, in carrying out for accumulating, especially this invention is a thing a hole like a contact hole is formed [a thing] in an insulating layer for dry etching and by which electrification of the conductive part is reduced compared with the former, even if the pars basilaris ossis occipitalis of a hole contacts a conductive part. Therefore, it supposes that a hole is divided and etched into multiple times like at least two steps, for example, before not reaching a conductive part at once, etching for hole formation is once stopped, and about subsequent etching, dry etching for hole formation in the condition of having formed the conductive layer in the field exposed including the side attachment wall of a hole is performed until a hole reaches a conductive part. Therefore, in the manufacture approach of a semiconductor device, this conductive part can reduce the bad influence by electrification of a conductive part by being altogether adapted, when forming a hole like a contact hole to a semiconductor region, wiring, etc. which are in the condition of floating. When forming a semiconductor device, for example, CMOS etc., in a SOI substrate, it uses and is suitable for formation of the hole for connection to semi-conductor layers, such as a conductive semi-conductor with which the source, the drain field, and metal wiring and an impurity were doped, and polish recon, etc.

[0033] (Gestalt of operation) As the manufacture approach of the semiconductor device using a SOI substrate, the example which forms CMOS is explained below with reference to drawing 1 . This drawing 1 is a sectional view which explains typically the process of the gestalt of implementation of the manufacture approach of the semiconductor device of this invention. In addition, in this drawing 1 , the same sign shows the part equivalent to the conventional example shown in drawing 2 .

[0034] As shown in drawing 1 (1), a SOI substrate is embedded on the support substrate 3, and has a silicone film 1 an oxide film 2 and on it. Since it is thick, in order to obtain SOI of high quality, this oxidizes the surface silicon layer 1 which forms a transistor, and it obtains the surface silicon layer of the support substrate 3 which is silicon by adjusting the thickness of the silicon layer 1 to 70nm using

etching etc. while it forms a silicon layer further. The thickness of an oxide film 2 is 100nm here.
[0025] Subsequently, an oxide film 4 is formed in 10nm thickness by the oxidizing [thermally] method, the SIN film (not shown) is formed in the thickness of 100nm by LPCVD (low-temperature chemical vapor deposition), and the photolithography method and dry etching remove the SIN film of a component isolation region, and an oxide film 4. Next, it oxidizes thermally by the thickness of 160nm, the oxidation for isolation and the film 5 are formed, and a heat phosphoric acid removes the SIN film (refer to drawing 1 (2)).
[0026] With the photolithography method and ion-implantation of a PMOS active region, the ion implantation of Lynn is carried out in impregnation energy 25KeV, and dose 5x1012 ion / cm2, and the high impurity concentration of the channel field 6 of PMOS is determined. Then, the ion implantation of the boron is carried out to an NMOS active region with the photolithography method and ion-implantation in impregnation energy 30KeV, and dose 5x1012 ion / cm2, and the high impurity concentration of the channel field 7 of NMOS is determined. Furthermore, HF removes an oxide film 4 1%, and gate oxide 8 is formed in the thickness of 7nm by the oxidizing [thermally] method. Then, the polish recon layer 9 is formed in the thickness of 150nm by the LPCVD method, the ion implantation of Lynn is carried out to the polish recon layer 9 with ion-implantation in impregnation energy 20KeV, and dose 5x1015 ion / cm2, and the WSi layer 10 is formed in the thickness of 100nm with a CVD method. Then, the WSi layer 10 and polish recon are etched by the photolithography method and the dry etching method, and a gate electrode is formed (refer to drawing 1 (3)).
[0027] The ion implantation of BF2 is carried out to a PMOS active region with the photolithography method and ion-implantation in impregnation energy 20KeV, and dose 5x1013 ion / cm2, and the high impurity concentration of the drain buffer diffusion layer 11 of PMOS is determined. In addition, since it is referred to as the so-called LDD, this drain buffer diffusion layer 11 is established. Then, the ion implantation of Lynn is carried out to an NMOS active region with the photolithography method and ion-implantation in impregnation energy 15KeV, and dose 5x1013 ion / cm2, and the high impurity concentration of the drain buffer diffusion layer 12 of NMOS is determined. Since it is referred to as the so-called LDD, this drain buffer diffusion layer is established. In order to use it, making the active-region section of PMOS and NMOS depletion-ize fundamentally, thickness is thinly formed in low concentration. Then, 150nm (not shown) of oxide films is formed with a CVD method, 140nm etchback of this oxide film is carried out by the dry etching method, and the sidewall 13 of an oxide film is formed in a gate electrode side attachment wall.
[0028] Then, the ion implantation of BF2 is carried out to a PMOS active region with the photolithography method and ion-implantation in impregnation energy 20KeV, and dose 5x1015 ion / cm2, and the source of PMOS and the high impurity concentration of the drain diffusion layer 14 are determined. Then, the ion implantation of Lynn is carried out to an NMOS active region by the photolithography method and the ion method in impregnation energy 15KeV, and dose 5x1015 ion / cm2, and the source of NMOS and the high impurity concentration of the drain diffusion layer 15 are determined (refer to drawing 1 (4)).
[0029] 150nm of NSG (non dope silicate glass) film 16 is formed by the applying method, and 750nm of BPSG (boron phosphorus silicate glass) film 17 is continuously formed by the applying method. In addition, the NSG film 16 and the BPSG film 17 form an interlayer insulation film. Then, 900 degrees C, nitrogen-gas-atmosphere mind, and the impurity that performed heat treatment for 20 minutes and carried out the ion implantation with the reflow of the BPSG film 16 and the above are activated. In this way, a source field and a drain field will be formed and, as for PMOS and an NMOS active region, the semiconductor device of PMOS and NMOS will be formed.
[0030] Then, the TiN layer 36 is formed in the thickness of 300nm by the spatter. In addition, as a conductive layer, although the example of TiN was given, the formation approach is not limited to a spatter and may be based on a CVD method, vacuum deposition, etc. here that what is necessary is just the conductive film which can be removed at a next process. If that thickness is not limited to this example and the resistance at the time of removal at a next process and contact etching is taken into consideration, its 200-400nm is desirable and its 250-300nm is especially desirable. Then, opening of

the contact hole section 19 for connecting electrode wiring with a semiconductor device by the photolithography method is formed in a resist 18 (refer to drawing 1 (5)).

[0033] The TiN layer 36 is etched into a mask for the resist 18 which carried out opening of the contact hole section 19 by dry etching. At this time, etching conditions of an etching system are BCL3 flow-rate 30sccm, Cl2 flow-rate 70sccm, degree of vacuum 8mTorr, 300mA of mu wave currents, and wafer maintenance electrode impression power 70W using mu wave plasma etching system, and the amount of over etching is made into 30% to the thickness of the TiN layer 36. Then, this resist 18 is used as a mask and opening of the contact hole 20 is used to the BPSG film 17 and the NSG film 16 by dry etching. Let the etching depth of the contact hole 20 of this ** be extent of a gate electrode which reaches up a little. Therefore, in a source field and the drain field upper part, this contact hole 20 is not formed in the depth of extent of a gate electrode located a little up, and does not arrive at a gate electrode, a source field, and a drain field. The etching system is impressing the RF also to a wafer maintenance electrode using an inductive-coupling mold plasma etching system. The etching condition is C2F6 flow-rate 50sccm, degree of vacuum 5mTorr, source impression power 2500W, and wafer maintenance electrode impression power 800W.

[0034] Then, a resist 18 is removed by the plasma ashing method, and organic exfoliation is performed (refer to drawing 2 (6)).

[0035] Subsequently, the TiN layer 37 is formed in the thickness of 20nm by the spatter. This film is not only TiN but conductive film, and that what is necessary is just what can be formed in the side attachment wall of a contact hole 20, the formation approach is not limited to a spatter, either and it may depend it on a CVD method and vacuum deposition. Although especially this thickness is not limited, its thickness of 5-30nm is desirable, and its about 10-30nm is especially good from the stability of the formation film etc. (refer to drawing 2 (7)).

[0036] Next, by the anisotropy dry etching method, TiN layer 37 part of the pars basilaris ossis occipitalis of a contact hole 20 is removed, and as the TiN layer 37 and the TiN layer 36 have a flow electrically, the sidewall of the TiN layer 37 is formed in the side attachment wall of a contact hole 20. At this time, etching conditions of an etching system are BCl3 flow-rate 30sccm, Cl2 flow-rate 70sccm, degree of vacuum 8mTorr, 300mA of mu wave currents, and wafer maintenance electrode power 70W using mu wave plasma etching system, and the amount of exaggerated etching is made into 20% to the thickness of the TiN film 37 of the pars basilaris ossis occipitalis of a contact hole 20. Furthermore, opening of the being [it / the oxide film which remains in the pars basilaris ossis occipitalis of a contact hole 20] BPSG film 17, and the NSG film 16 is carried out by dry etching (refer to drawing 2 (8)). At this time, the etching system is impressing the RF also to a wafer maintenance electrode using an inductive-coupling mold plasma etching system. Etching conditions are C2F6 flow-rate 50sccm, degree of vacuum 5mTorr, source impression power 2500W, and wafer maintenance electrode impression power 800W. Since the TiN layer 37 which flows electrically in the TiN layer 36 exists in the side attachment wall of a hole 20 as a sidewall during this etching, electrification of the side attachment wall of a hole 20 is reduced compared with the former. Consequently, although the source and the drain field to which contact hole 20 pars basilaris ossis occipitalis is made into the active region with advance of dry etching are arrived at, electrification of the active region of the pars basilaris ossis occipitalis is eased compared with the former, the potential difference between an active region and a support substrate also becomes small compared with the former, and degradation of the embedding oxide film 2 is prevented.

[0037] Next, **** to the solution of a 150-degree C sulfuric acid and hydrogen peroxide solution removes the TiN layers 37 and 36. In addition, since a substrate semi-conductor (the source, the drain field which are an active region) received a damage if dry etching performs hole dawn, wet etching was performed for preventing this here. Then, Ti is formed by the thickness of 60nm by the spatter, TiN is continuously formed by the thickness of 60nm, and the barrier metal layer 21 is formed. Furthermore, with a CVD method, 22 [W-layer] is formed by the thickness of 500nm, the etching back of 22 [W-layer] is carried out by the dry etching method, and it leaves 22 [W-layer] only to the part of a contact hole 20. Next, etchback of the barrier metal layer 21 is carried out by the dry etching method, and it

leaves the barrier metal 21 only to contact hole 20 part. subsequently, a spatter -- with the thickness of 80nm, the AlCu layer 24 (0.5% of Cu concentration) is carried out by the thickness of 400nm, and sequential formation of the TiN layer 25 is carried out for the TiN layer 23 by the thickness of 80nm. Then, by the photolithography method and the dry etching method, the TiN layer 25, the AlCu layer 24, and the TiN layer 23 are etched, and electrode wiring is formed (refer to drawing 3 (9)).

[0036] a plasma-CVD method -- SiO two-layer -- 26 -- the thickness of 2 micrometers -- forming -- continuing -- the CMP method -- SiO two-layer -- flattening of 26 is carried out. here -- the SiO two-layer after CMP -- the thickness of 26 is on electrode wiring and is set to 1 micrometer. In addition, this SiO two-layer 26 becomes an interlayer insulation film. Then, the TiN layer 38 is formed by the thickness of 300nm by the spatter. This film is not limited to TiN, and that what is necessary is just the conductive film removable at a next process, the formation approach is not limited to a spatter, either and it is easy to depend it on a CVD method, vacuum deposition, etc. Although especially the thickness is not limited, if removal at a back process, the stability of the formation film, etc. are taken into consideration, its 200-400nm is desirable, and its 250-300nm is especially desirable. Subsequently, opening of the veer hole section 28 which connects electrode wiring and up electrode wiring by the photography method is formed in a resist 27 (refer to drawing 3 (10)).

[0037] The TiN layer 38 is etched by performing dry etching for the resist 27 which carried out opening of this veer hole section 28 on a mask. In the etching system, etching conditions make the amount of exaggerated etching 30% to the thickness of the TiN layer 38 using mu wave plasma etching system by BCl3 flow-rate 30sccm, Cl2 flow-rate 70sccm, degree of vacuum 8mTorr, 300mA of mu wave currents, and wafer maintenance electrode impression power 70W. Then, opening of the veer hole 29 is carried out to SiO2 film 26 which is an interlayer insulation film by carrying out dry etching of this resist 27 to a mask. It is made even for electrode wiring not to attain the etching depth of the veer hole 29 at this time (drawing 4 (11 (reference).)). The etching system is impressing the RF also to a wafer maintenance electrode using an inductive-coupling mold plasma etching system. Etching conditions are C2F6 flow-rate 50sccm, degree of vacuum 5mToor, source impression power 2500W, and wafer maintenance electrode impression power 800W.

[0038] Then, a resist 27 is removed by the plasma ashing method, and organic exfoliation is performed. Subsequently, the TiN layer 39 is formed in the thickness of 10nm by the spatter (refer to drawing 4 (12)). At this time, that what is necessary is just what can be formed in the side attachment wall of the veer hole 28 not only by TiN but by the conductive film, the formation approach is not limited to a spatter, either and the film 38 may depend it on a CVD method, vacuum deposition, etc. Although especially this thickness is not limited, its 5-30nm is desirable, and its about 10-30nm is especially good from the stability of the formation film etc.

[0039] Next, by the anisotropy dry etching method, the remaining TiN layers 39 of the pars basilaris ossis occipitalis of the veer hole 29 are removed, and as the TiN layer 38 and the TiN layer 39 have a flow electrically, the sidewall of the TiN layer 39 is formed in the side attachment wall of the veer hole 29. Etching conditions of an etching system are BCl3 flow-rate 30sccm, Cl2 flow-rate 70sccm, degree of vacuum 8mTorr, 300mA of mu wave currents, and wafer maintenance electrode impression power 70W using mu wave plasma etching system, and the amount of exaggerated etching is made into 20% to the thickness of the TiN layer 39 of veer hole 29 pars basilaris ossis occipitalis. Furthermore, opening of the part in which the oxide film (SiO2 film 26) of the pars basilaris ossis occipitalis of the veer hole 29 remains is carried out by dry etching (refer to drawing 5 (13)). The etching system is impressing the RF to a wafer maintenance electrode using an inductive-coupling mold plasma etching system. Etching conditions are C2F6 flow-rate 50sccm, degree of vacuum 5mTorr, source impression power 2500W, and wafer maintenance electrode impression power 800W. Since the TiN layer 38 and the TiN layer 39 which flows electrically exist in the side attachment wall of the veer hole 29 as sidewalls during this etching, electrification of the side attachment wall of the veer hole 29 is reduced compared with the former. Consequently, although the TiN layer 25 in which the pars basilaris ossis occipitalis of the veer hole 29 makes electrode wiring with advance of dry etching is reached, electrification of electrode wiring of the pars basilaris ossis occipitalis is eased compared with the former, the potential difference

between electrode wiring and a support substrate also becomes small compared with the former, and degradation of the embedding insulator layer 2 is prevented. Subsequently, the TiN layers 39 and 38 are removed. Next, Ti layer is formed in the thickness of 60nm by the spatter, a TiN layer is continuously formed in the thickness of 60nm by the spatter, and the barrier metal layer 30 is formed. Next, 31 [W-layer] is formed in the thickness of 500nm with a CVD method, the etching back of 31 [W-layer] is carried out by the dry etching method, and it leaves 31 [W-layer] only to the veer hole 29 section. Next, etchback of the TiN layer 38 and the barrier metal layer 30 is carried out by the dry etching method, and it leaves the barrier metal layer 30 only to the veer hole 29 section (refer to drawing 5 (14)).

[0040] next, SUPPATA -- law -- the TiN layer 32 -- the AlCu layer 33 (0.5% of Cu concentration) is formed in the thickness of 80nm at the thickness of 800nm, and the TiN layer 34 is formed in the thickness of 80nm in order. Then, by the photolithography method and the dry etching method, the TiN layer 34, the AiCu layer 33, and the TiN layer 32 are etched, and up wiring is formed. Then, SiN film 35 of the passivation film is formed in the thickness of 600nm by the plasma-CVD method (refer to drawing 6 (15)). Then, opening of the Bondi GUPADDO connection hole is carried out to the SiN layer 35 by the photolithography method and the dry etching method.

[0041] Proof-pressure distribution of the embedding oxide film at the time of manufacturing according to the manufacturing method of the gestalt of operation of this invention is shown in drawing 11 (1), and proof-pressure distribution of the embedding oxide film at the time of manufacturing according to the conventional manufacturing method is shown in drawing 11 (2), respectively. In drawing 11 , a proof pressure (MV/cm) is shown on an axis of abscissa, and frequency (%) is shown on the axis of ordinate. This drawing 11 shows decreasing sharply with 6% to being 63% by what the manufacturing method of this invention used at the thing of the manufacturing method of the former [destruction / of 1 or less MV/cm of proof pressures / initial].

[0042] Although the manufacture approach of the semiconductor device of this invention explained the example of the manufacture approach of a semi-conductor of having used the SOI substrate as a gestalt of the operation, it is applicable to the contact formation to the dry etching for contact formation in the semi-conductor layer of not only this but a flow TIGU condition, or a conductor layer, for example, the FUROTIN gate of memory, etc.

[0043]

[Effect of the Invention] Opening of the manufacture approach of the semiconductor device of this invention is carried out to extent which does not reach said the 1st conductive film and said insulator layer by etching at the conductive field of said semiconductor device, or said wiring. From forming the 2nd conductive film in the side attachment wall of the account opening of back to front, and forming a hole by carrying out opening of the conductive field of said semiconductor device, or said insulator layer after said wiring by dry etching in the condition of having made it flowing through the 2nd conductive film electrically with said 1st conductive film From the ability of electrification of the pars basilaris ossis occipitalis to be reduced compared with the former, even if it reaches a conductive field or wiring, the pars basilaris ossis occipitalis of a hole It is size the place which can be useful to prevention of degradation by dielectric breakdown of the insulator layer of a SOI substrate, can improve the electric withstand voltage of this insulator layer compared with the former, and contributes to the improvement in dependability of a semiconductor device.

[0044] after [furthermore,] formation of said hole etches said 1st conductive layer into a mask for the photoresist formed on said 1st conductive film -- this photoresist -- removing -- continuing -- this -- since a hole can be formed in self align from performing the 1st conductive film on a mask by carrying out dry etching of said insulator layer, it can manufacture with a sufficient precision and the semiconductor device of the stable engine performance can be obtained.

[0045] Moreover, it sets to the manufacture approach of the semiconductor device which carries out opening of the contact hole for forming the electrical installation to the semi-conductor or the conductive field by which insulating separation was carried out spatially to an insulating layer by etching. By performing plasma etching and forming a contact hole until it arrives at said field, where a conductive layer is formed in the field which said insulating layer exposes including the side-

attachment-wall section of opening which formed etching by the stop and after that etching before arriving at said field From the ability of electrification of the pars basilaris ossis occipitalis to be reduced compared with the former, even if the pars basilaris ossis occipitalis of a contact hole arrives at a semiconductor or a conductive field by plasma etching By being able to mitigate the bad influence to layers, such as an insulating layer by electrification, being able to prevent degradation of the property of equipment, and removing said conductive layer by wet etching, after forming a contact hole further Compared with dry etching, the bad influence to the substrate of the lower part of the contact hole can be reduced, and it contributes to obtaining equipment with a sufficient property.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The process which forms an insulator layer in the manufacture approach of the semiconductor device using a SOI substrate on wiring which connects a semiconductor device or it, and forms the 1st conductive film subsequently to the insulator layer top, Opening is carried out to extent which does not reach said the 1st conductive film and said insulator layer by etching at the conductive field of said semiconductor device, or said wiring. The 2nd conductive film is formed in the side attachment wall of the account opening of back to front. The manufacture approach of the semiconductor device characterized by having the process which forms a hole by carrying out opening of the conductive field of said semiconductor device, or said insulator layer after said wiring by dry etching in the condition of having made it flowing through the 2nd conductive film electrically with said 1st conductive film.
[Claim 2] after formation of said hole etches said 1st conductive layer into a mask for the photoresist formed on said 1st conductive film -- this photoresist -- removing -- continuing -- this -- the manufacture approach of the semiconductor device according to claim 1 characterized by performing the 1st conductive film by carrying out dry etching of said insulator layer at a mask.
[Claim 3] In the manufacture approach of a semiconductor device of having the process which carries out opening of the contact hole for forming the electrical installation to the semi-conductor or the conductive field by which insulating separation was carried out spatially to an insulating layer by etching Before arriving at said field, said process etching A stop, The manufacture approach of the semiconductor device characterized by performing plasma etching and forming a contact hole until it arrives at said field, where a conductive layer is formed in the field which said insulating layer exposes including the side-attachment-wall section of opening formed by etching after that.
[Claim 4] The manufacture approach of the semiconductor device according to claim 3 characterized by having the process which removes said conductive layer by wet etching after forming a contact hole according to said process.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the semiconductor device of this invention.
[Drawing 2] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the semiconductor device of this invention.
[Drawing 3] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the semiconductor device of this invention.
[Drawing 4] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the semiconductor device of this invention.
[Drawing 5] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the semiconductor device of this invention.
[Drawing 6] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the semiconductor device of this invention.
[Drawing 7] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the conventional semiconductor device.
[Drawing 8] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the conventional semiconductor device.
[Drawing 9] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the conventional semiconductor device.
[Drawing 10] It is the sectional view which explains typically the production process of the gestalt of implementation of the manufacture approach of the conventional semiconductor device.
[Drawing 11] It is a drawing explaining the electric withstand voltage property of the component manufactured by the manufacture approach of this invention and the conventional semiconductor device.
[Description of Notations]
1 [ ] Support Substrate
2 [ ] Embedding Oxide Film
3 [ ] Silicone Film
4 Five Oxide film
8 [ ] Gate Oxide
9 [ ] Polish Recon Layer
13 [ ] Sidewall
16 [ ] NSG Film
17 [ ] BPSG Film
18 27 Resist
20 [ ] Contact Hole
21 [ ] Barrier Metal Layer
22 [ ] W Layers

23, 25, 32, 34, 36, 37, 38, 39 TiN layer
24 33 AlCu layer
26 [ ] SiO2 Film
29 [ ] Veer Hole
35 [ ] SiN Film

[Translation done.]

* NOTICES *

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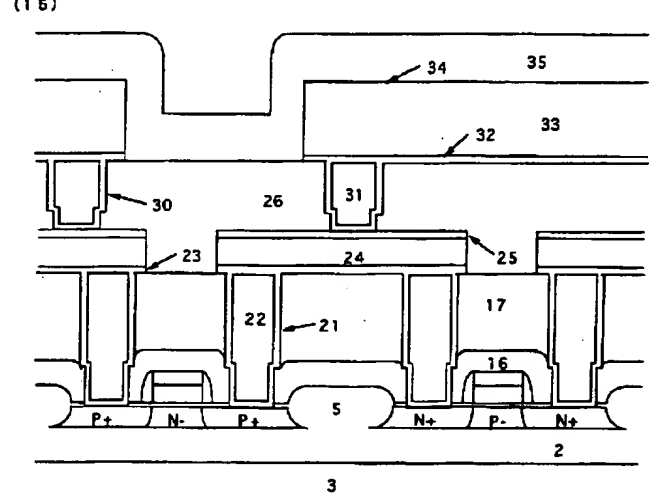
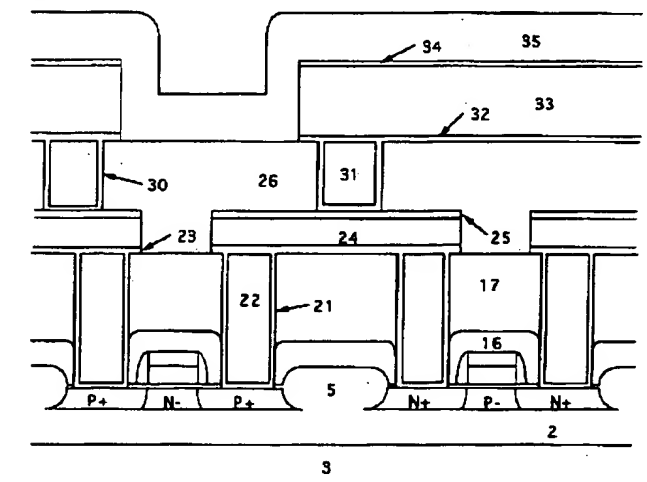
DRAWINGS

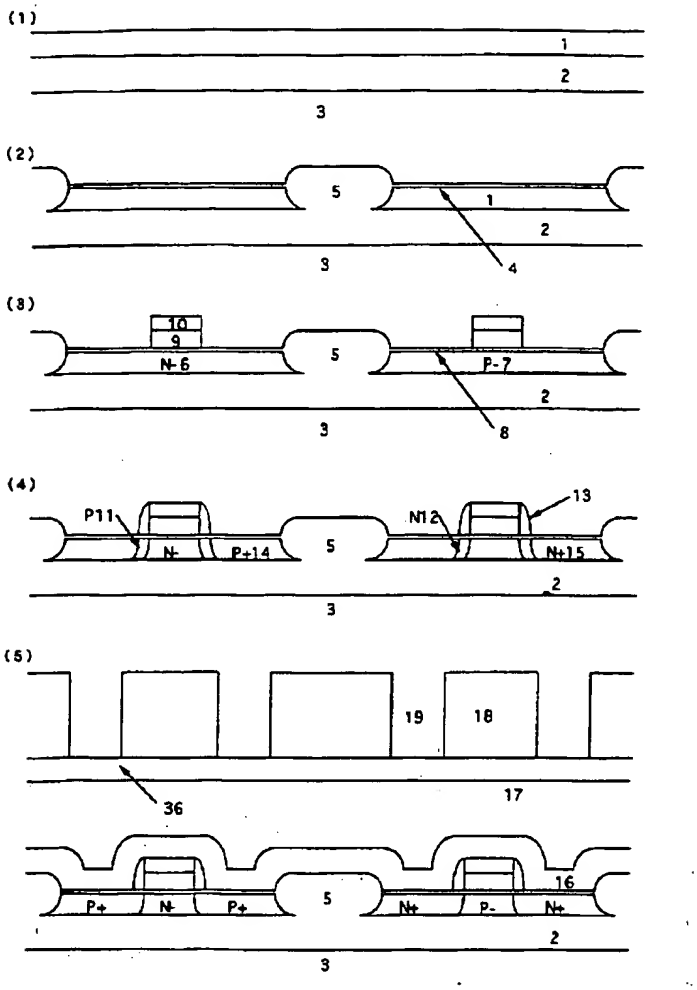
[Drawing 6]



[Drawing 10]



[Drawing 1]



[Drawing 2]

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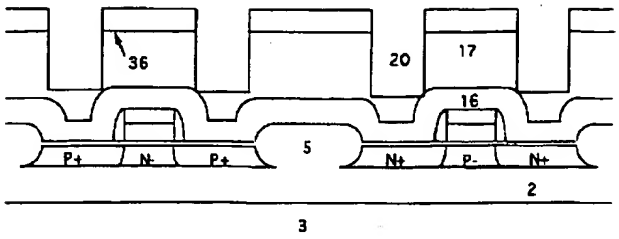

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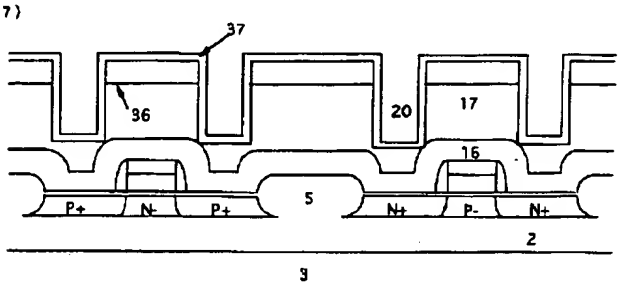

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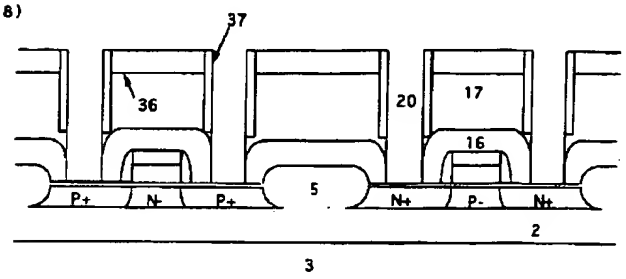

[Drawing 8]

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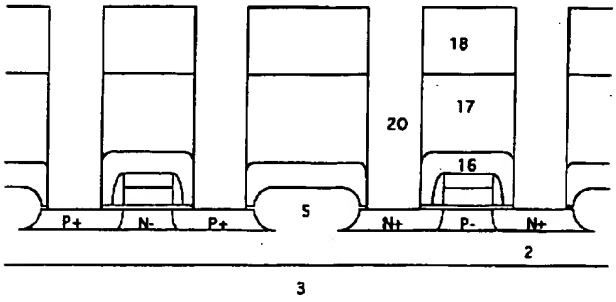

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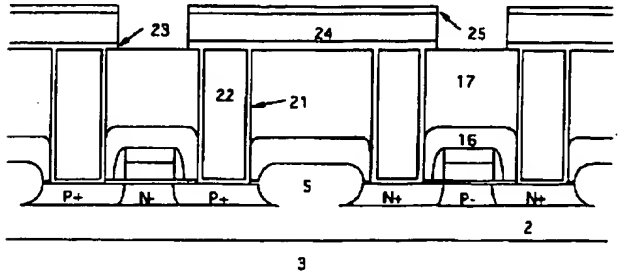

[Drawing 3]

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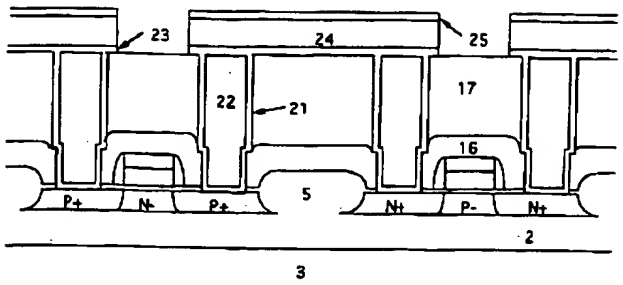

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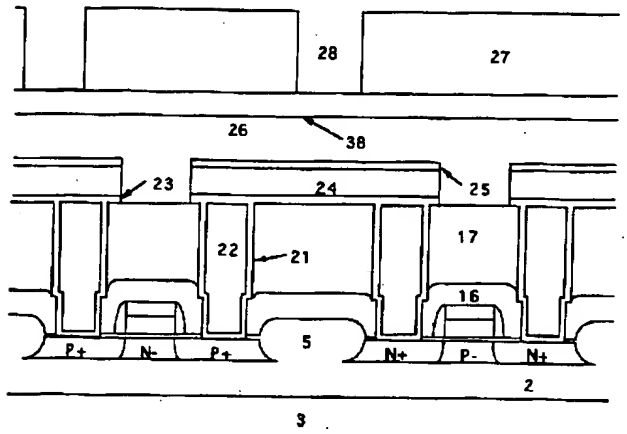
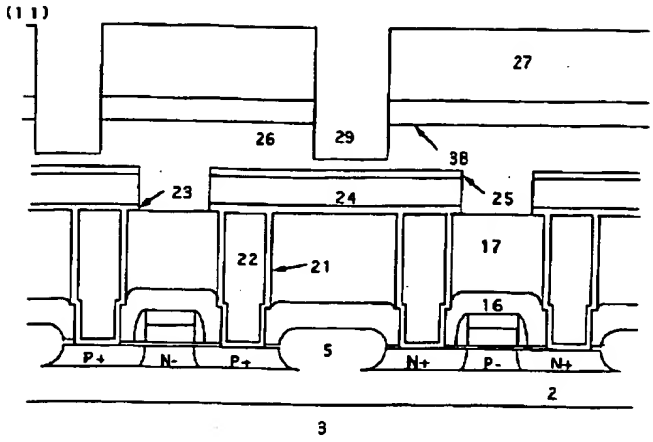
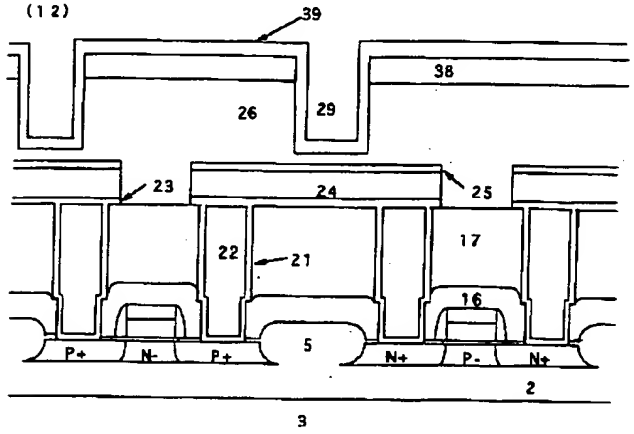
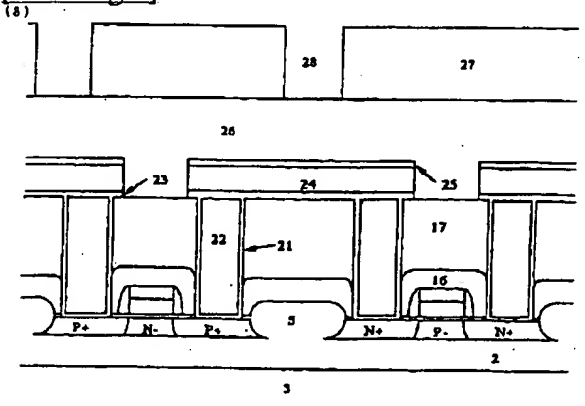


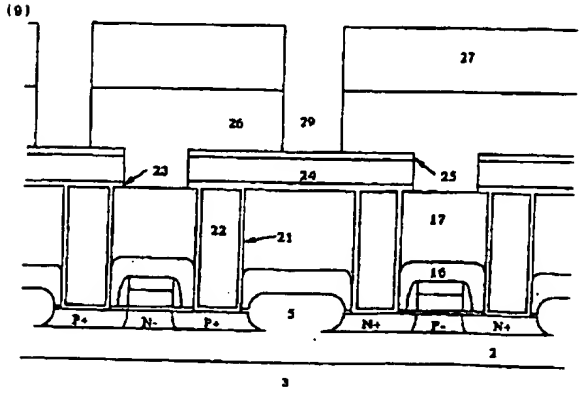
[Drawing 4]



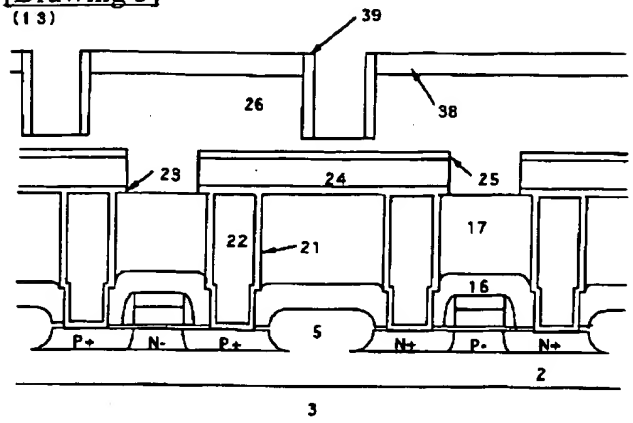


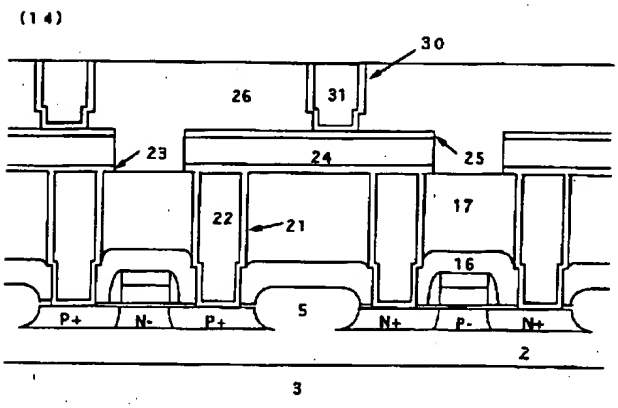
[Drawing 9]



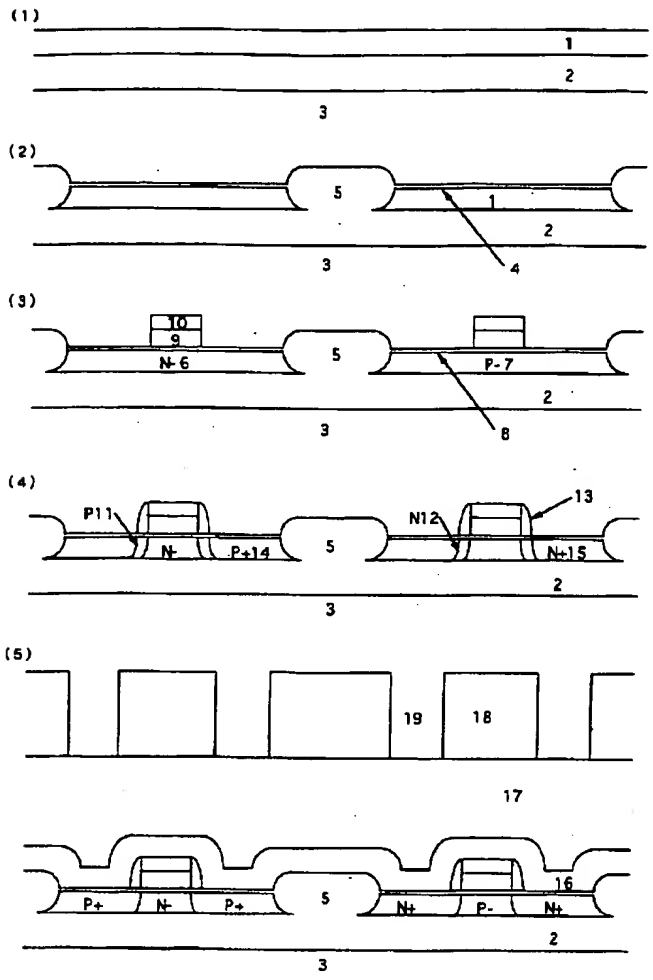


[Drawing 5]



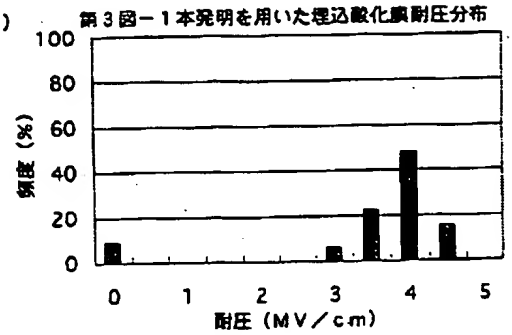


[Drawing 7]

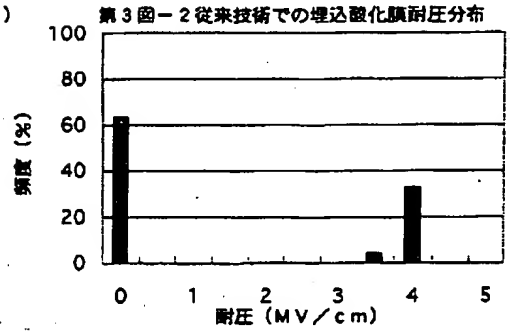


[Drawing 11]

(1) 第３図－１本発明を用いた埋込酸化膜耐圧分布



(2) 第３図－２従来技術での埋込酸化膜耐圧分布



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